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期末课程评教入口二维码

EE115B *Digital Circuits*

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Field Programmable Gate Array

Part 1: Concepts

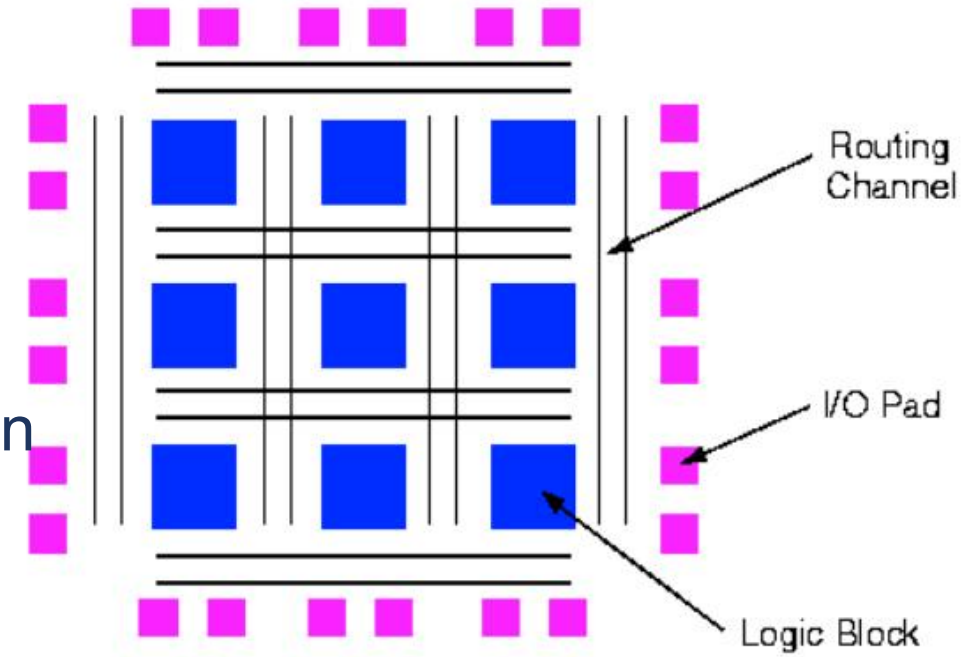
(Most contents in this part will not appear in exam, except for concepts that are very fundamental)

FPGA Introduction

First introduced by Xilinx in 1985.

Key Features:

- Arrays of logic blocks (to implement logic functions).
- Lots of programmable wiring in routing channels.
- Very flexible I/O interfacing logic core to outside world.



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AMD Xilinx FPGA series

- Zynq：Flexibility (FPGA + ARM CPU SoC),
- Virtex：High performance, highest logic density, flagship tier.
- Kintex： Mid-to-high performance, best price/performance ratio.
- Artix：Mid performance, low power/low cost applications.
- Spartan：Low performance, lowest cost.
- Versal：ACAP (Adaptive Compute Acceleration Platform=ARM+PL+AI Engine) - AI acceleration.

AMD Xilinx FPGA series

Fabrication Technology

- 45nm / 28nm / 16nm / 7nm... directly affecting integration density, power consumption, and frequency.

Resources

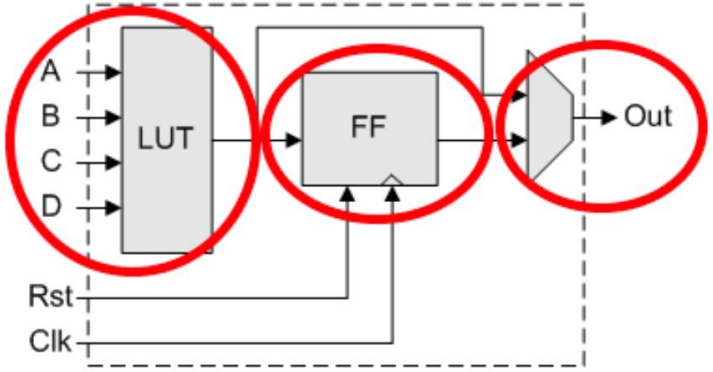
- **Logic Elements (LEs)**: Basic programmable units (>500K in high-end).
- **Memory: Block RAM (BRAM)** for general storage; UltraRAM (URAM) for high-bandwidth memory.
- **DSP Slices**: For heavy math and signal processing.
- **High-Speed Interfaces**: PCIe, Gigabit Ethernet transceivers.
- **Clocking Infrastructure**: PLLs, MMCMs.
- **SoC**: Hard-core CPUs (e.g., ARM Cortex in Zynq).

Resources: Logic Elements

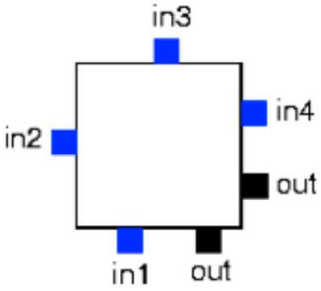
Logic Elements

- generally refers to 4-input LUT followed by FF
- (the newer Xilinx families all use 6 input LUTs)

- Based around Look-up Tables (LUTs), most common with 4-inputs
- Optional D-flipflop at the output of the LUT
- 4-input LUT can implement ANY 4-input Boolean equation (truth-table)
- Special circuits for cascading logic blocks (e.g. carry-chain of a binary adder)



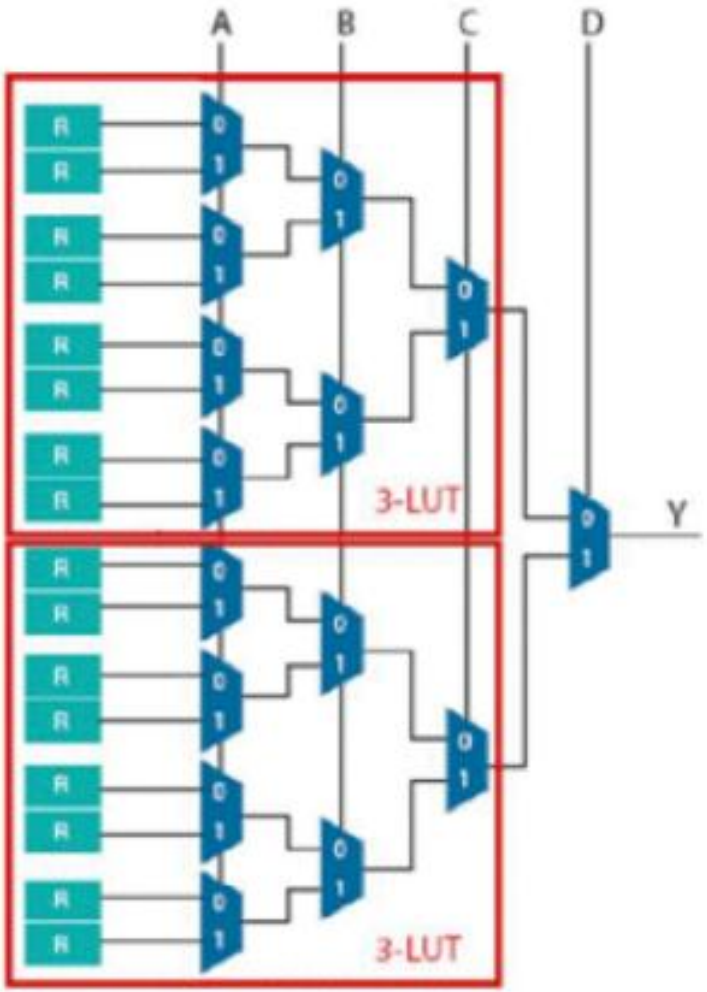
Logic Element (LE)



- Each logic block has pins located for easy access:

Resources: LUT

- Programming an FPGA is NOT the same as programming a microprocessor
- We download a **BITSTREAM** (not a program) to an FPGA
- Programming an FPGA is known as **CONFIGURATION**
- All LUTs are configured using the BITSTREAM so that they contain the correct values to implement the Boolean logic
- Shown here is a typical implementation of a 4-LUT circuit
  - ABCD are the FOUR inputs
  - There is four level of 2-to-1 multiplexer circuits
  - The 16-inputs to the mux tree determine the Boolean function to be implemented as in a truth-table
  - These 16 binary values are stored in registers (DFF)
  - Configuration = setting the 16 registers to 1 or 0



R is a register that stores either 1 or 0. For example, if ABCD=0000, then the first R is routed to Y.

Resources: Programmable Interconnect

- Switch matrices & routing channels connect CLBs, BRAM, and DSP slices together.
- The Routing Delay Problem: In modern FPGAs, the delay caused by wires is often longer than the delay of the logic gates themselves!
- Critical for Timing Closure (ensuring the design meets the target clock frequency).
- Can be optimized by writing efficient code, or applying physical Placement & Routing (P&R) constraints to group related logic close together.
- Routing resources: wires and switches (antifuse or pass transistors)
- Global Clock Line：optimized tree-structured path that ensures high accuracy time alignment.

Resources: RAM Blocks

Distributed RAM: Small memories built using the LUTs inside normal CLBs. Good for very small FIFOs or shift registers.

Block RAM (BRAM): Dedicated 18/36 Kb SRAM memory blocks physically embedded in the silicon.

- Supports single-port, dual-port, and FIFO modes.
- Used for data buffering, large lookup tables, and image/video line buffers.

UltraRAM (URAM): Only available in newer/larger families. Massive volume storage (288 Kb blocks) to replace external SRAM chips.

Resources: DSP Slices

DSP: Digital Signal Processing. Using LUTs to build a 48-bit multiplier consumes massive resources and is very slow. DSP slices do it in one clock cycle.

Function: High-speed multipliers & accumulators (MAC operations). Used in filters, FFTs, and matrix operations.

Example: A DSP48E1 slice can perform (A × B) + C in one cycle with a 48-bit accumulator width.

Resources: MMCM & PL (Clock Management)

Phase-Locked Loop (PLL):

- Used for simpler clock generation. Can multiply a slow input clock to a fast internal clock (e.g., 50MHz in → 200MHz out).

Mixed-Mode Clock Manager (MMCM):

Xilinx's advanced version of a PLL.

- Provides advanced jitter filtering.
- Allows phase shifting (e.g., shifting a clock by 90 degrees to align with DDR data).
- Used for deskewing and safe Clock Domain Crossing (CDC).

Resources: IOB

Definition: IOBs are the programmable interfaces between the internal FPGA logic (CLBs) and the physical external pins.

Key Components:

I/O Buffers (IBUF/OBUF): Programmable to support different voltage standards (LVCMOS33, LVDS, etc.).

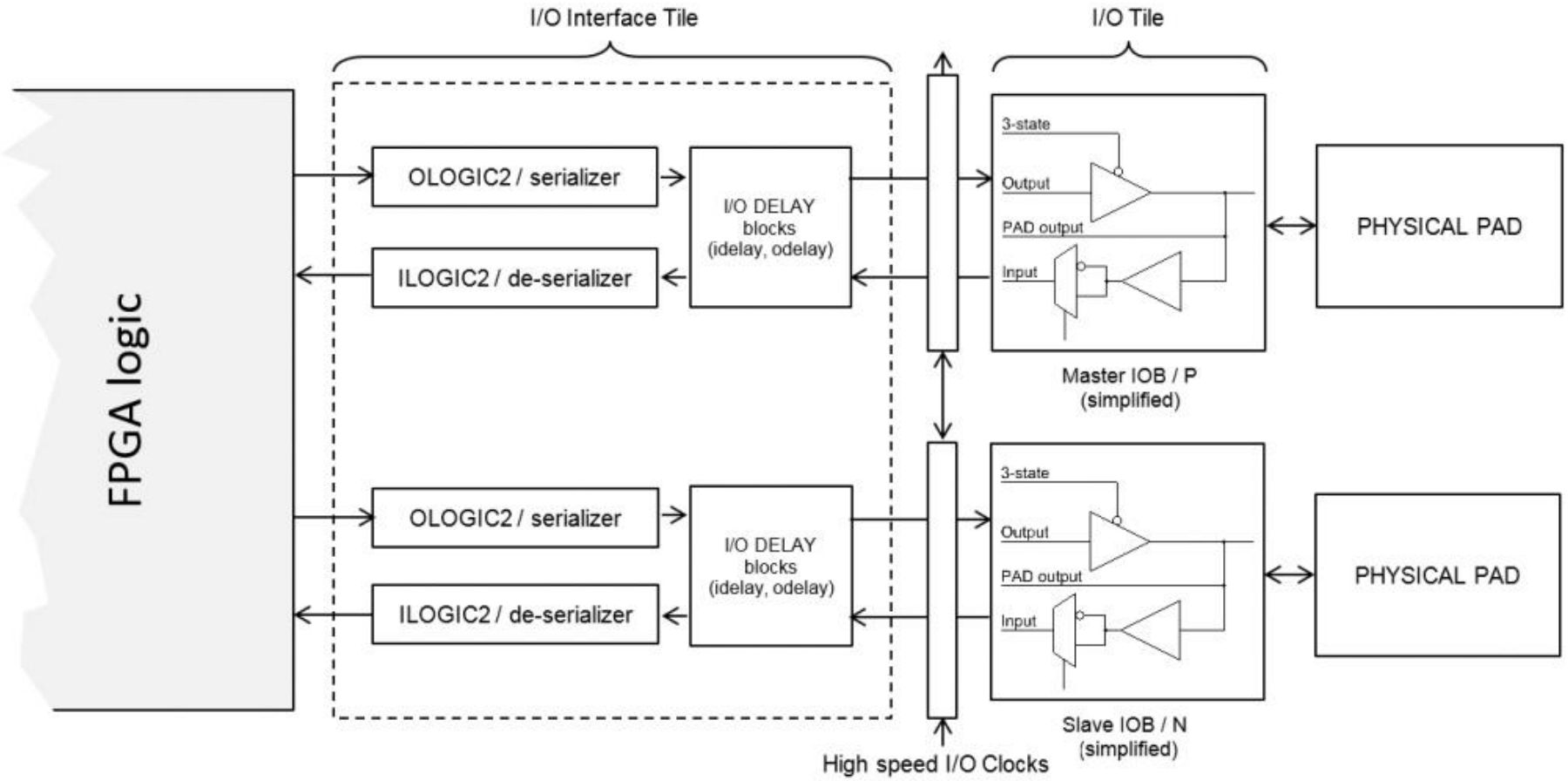
Tristate Control (OBUFT): Allows pins to act as bidirectional inputs/outputs (e.g., I2C lines).

I/O Registers (IDDR/ODDR): Dedicated Flip-Flops placed right next to the physical pin to guarantee fast, predictable "Clock-to-Out" and "Setup/Hold" times.

Programmable Resistors: Internal Pull-up or Pull-down resistors.

Resources: IOB

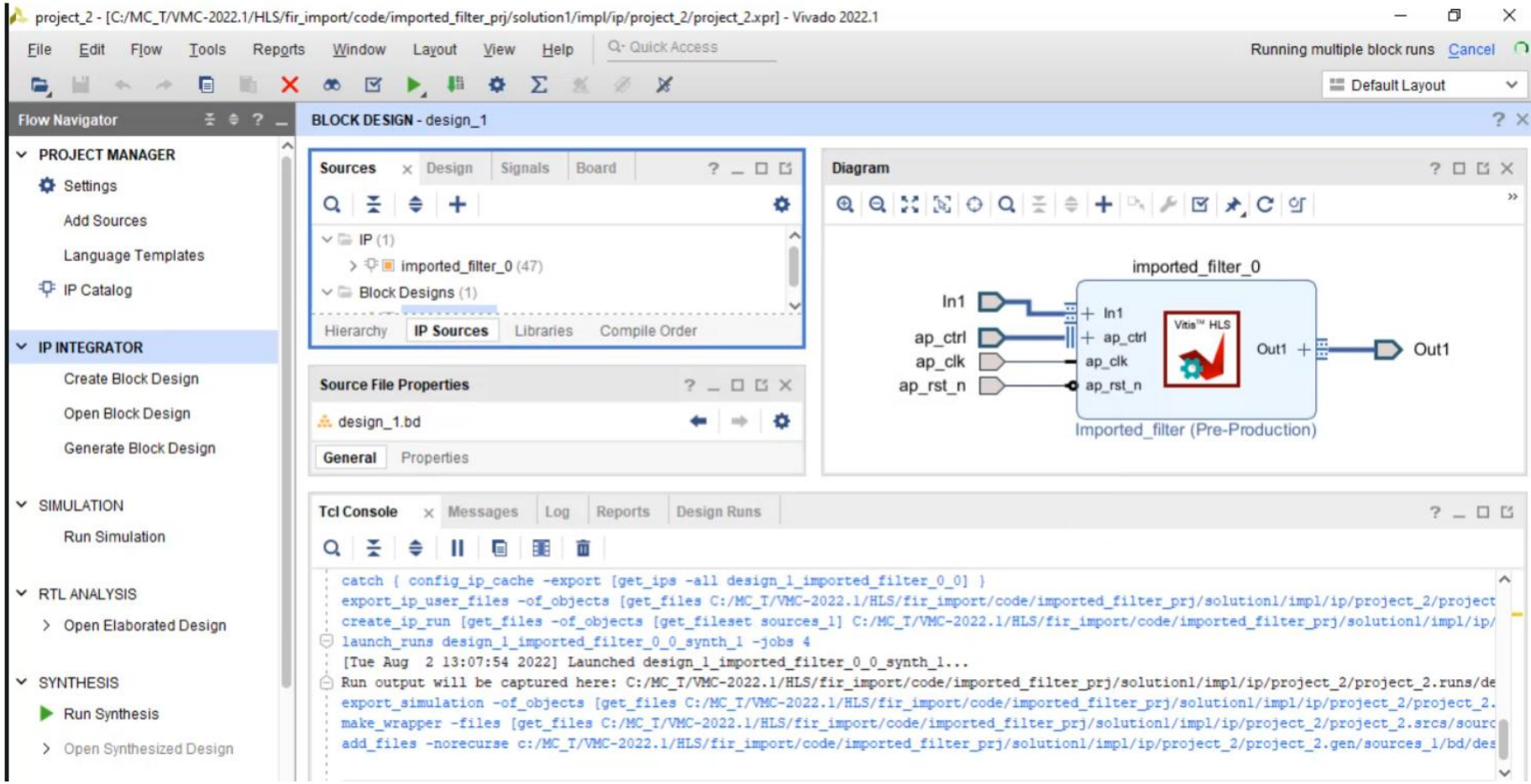
https://fp-instruments.com/en/how-fpgas-input-output-blocks-can-reduce-pcb-complexity/



Development Workflow

- **Design Entry:** Write RTL (Verilog / SystemVerilog) or use Block Design (IP Integrator).
- **Simulation:** Run a testbench to verify logic behavior before hardware synthesis (e.g., Vivado Simulator).
- **Synthesis:** Tool converts your Verilog code into fundamental FPGA elements (LUTs, FFs).
- **Implementation (Place & Route):** Tool maps the elements to physical locations on the chip and routes the microscopic wires between them.
- **Timing Analysis:** Verifies if the routed design can run at your requested Clock Speed.
- **Bitstream Generation:** Compiles the design into a .bit file.
- **Hardware Programming:** Download to the board via USB/JTAG.

Development Workflow



https://www.mathworks.com/videos/getting-started-with-the-avnet-zuboard-part-3-elaborate-the-design-using-vivado-1661496543633.html

Development Methods

RTL (Register Transfer Level): The industry standard. Uses Verilog, VHDL, or SystemVerilog. Gives the engineer exact, cycle-by-cycle control over hardware timing.

High-Level Synthesis (HLS): Writing algorithms in C/C++. Vivado HLS translates C code into Verilog automatically. Great for complex math, but abstracts away timing control.

IP Block Design: Dragging and dropping pre-built modules (UART, Memory Controllers, CPU cores) via Vivado IP Integrator.

Third-Party Tools: Matlab/Simulink HDL Coder, LabVIEW FPGA (used highly in testing/RF).

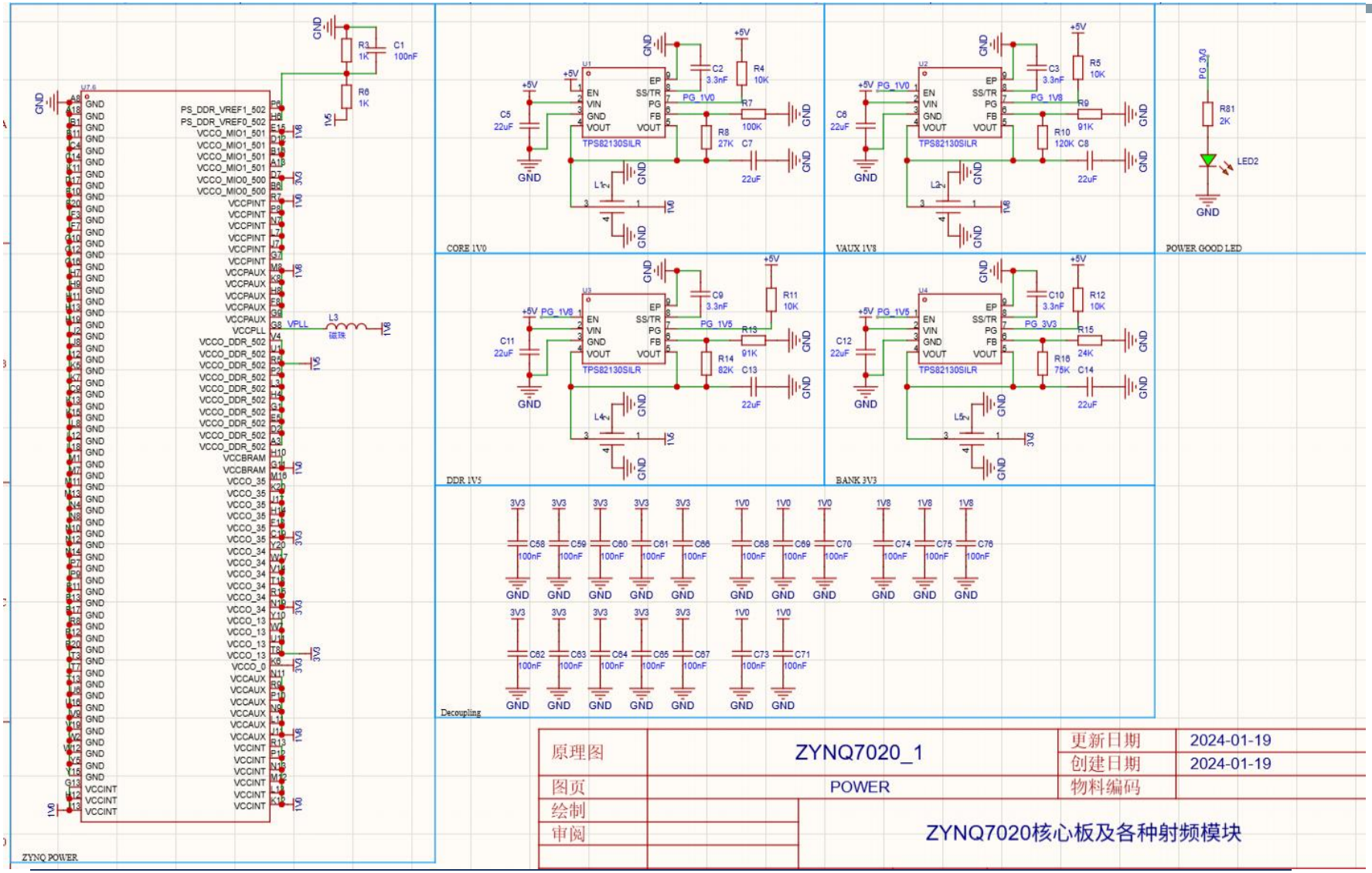
AI EDA Design: Large Language Model for coding/optim/...

Field Programmable Gate Array

Part 2: Hardware Circuits

(This part will not appear in exam)

FPGA hardware design: POWER CIRCUIT

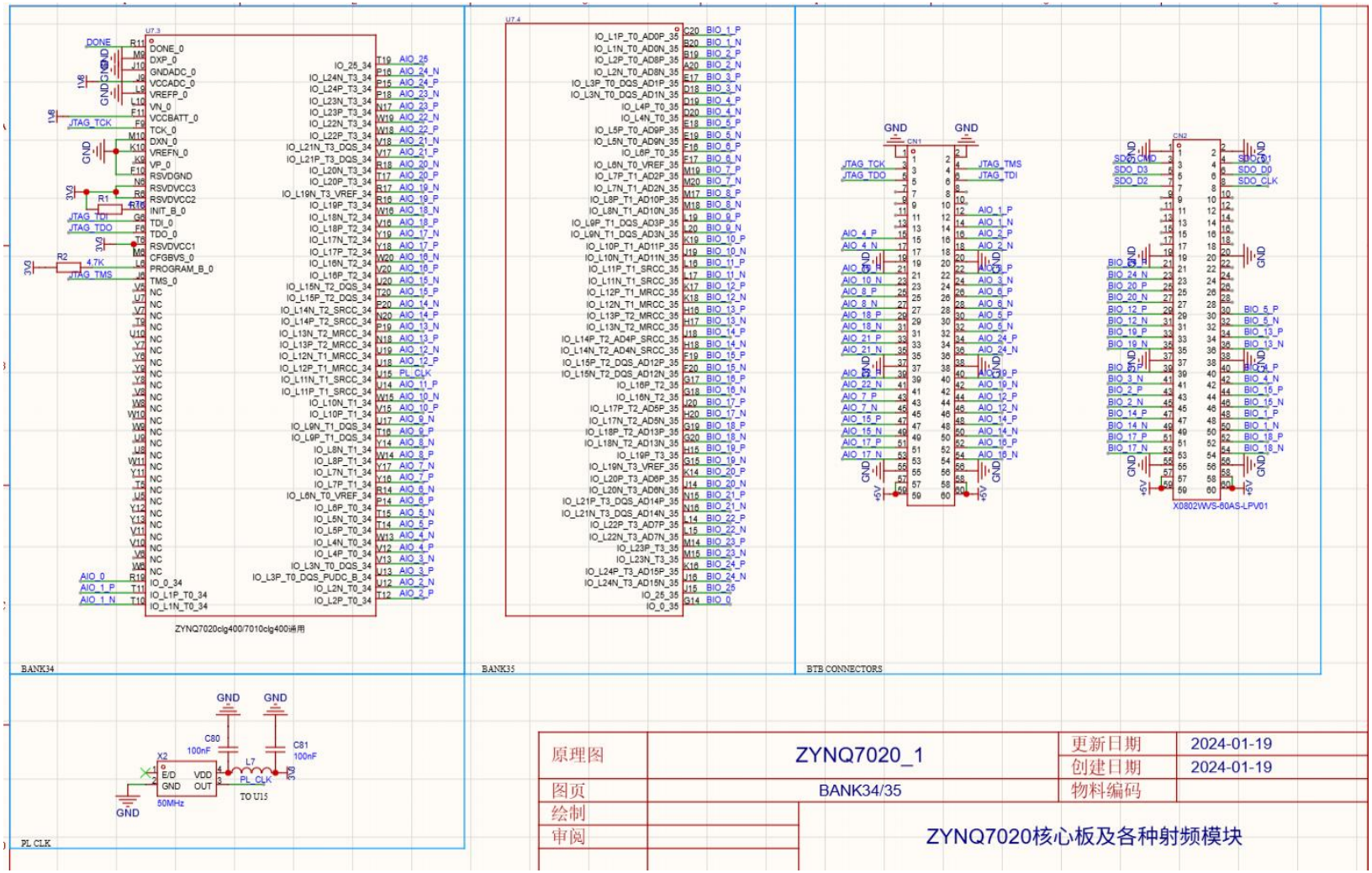


https://oshwhub.com/z_star/zynq7020-core-board-and-various-rf-modules

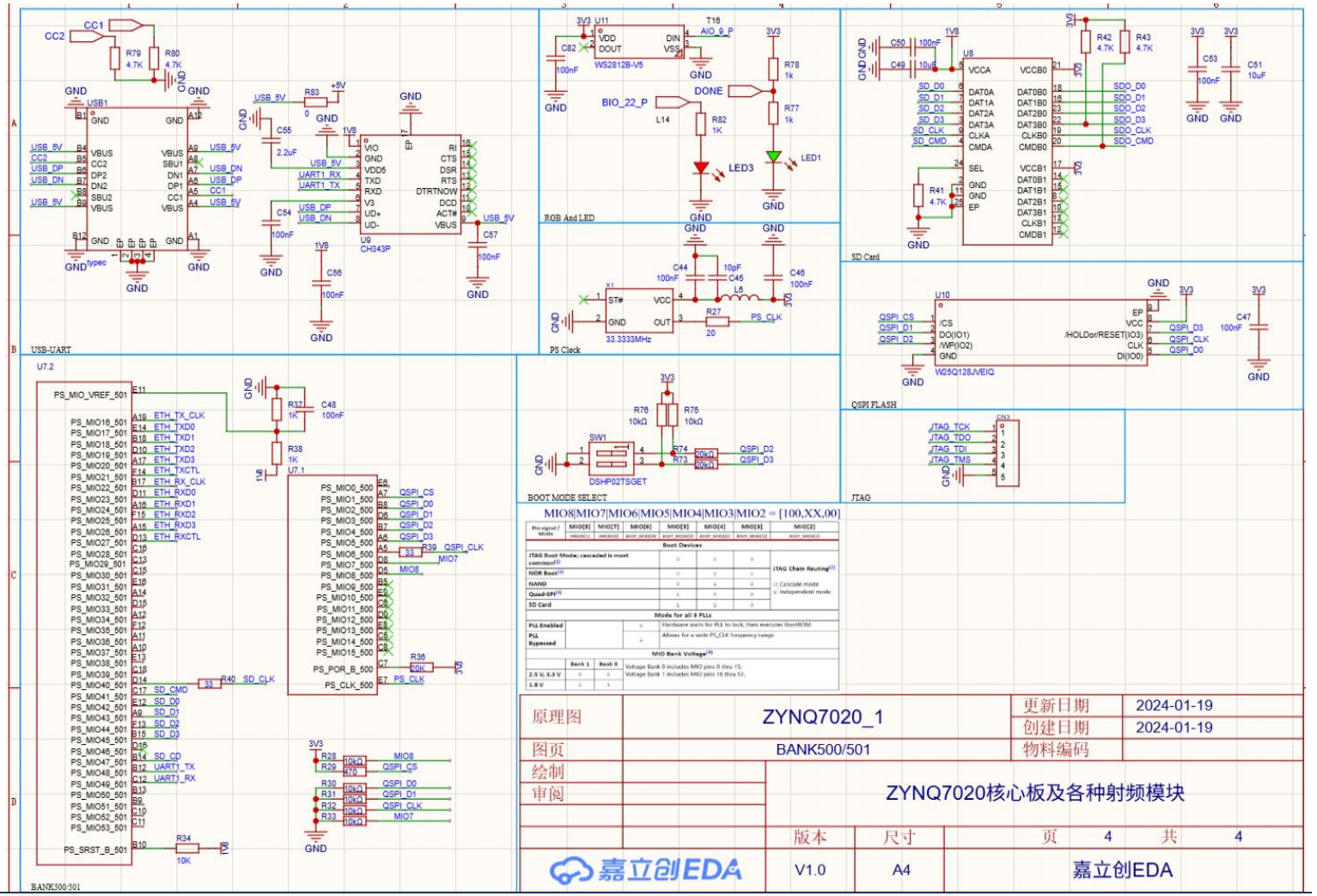
FPGA hardware design: Power Supplies

- VCCINT: Core logic power supply (typically 1.0 V) Powers internal routing and LUTs.
- VCCBRAM: Block RAM power supply (typically 1.0 V)
- VCCAUX: Auxiliary power supply (e.g., PLLs and configuration logic) (e.g., 1.8V for PLLs, JTAG, and configuration logic).
- VCCO_XXXX: I/O bank power supply (voltage depends on I/O standard) (e.g., 3.3V, 2.5V, 1.8V).
- VCCBAT: Battery backup supply (for configuration and real-time clock)
- VCCADC: ADC power supply
- Power Sequencing: Power supplies must be turned on in a specific order (usually VCCINT → VCCAUX → VCCO) to prevent massive current spikes and device damage.

FPGA hardware design: IO BANKS



FPGA hardware design: IO BANKS



https://oshwhub.com/z_star/zynq7020-core-board-and-various-rf-modules

FPGA hardware design: Configuration & Boot

Configuration & Boot

- PROGRAM_B: Forces device reconfiguration when asserted
- INIT_B: Indicates initialization status and configuration errors
- DONE: Goes high when configuration is successfully completed
- MODE[ ]: Selects configuration mode (JTAG, QSPI, SD, etc.)

FPGA hardware design: Clock

Clocking

- GCLK / MRCC / SRCC: Global and regional clock input pins
- REFCLK: Reference clock input for high-speed transceivers

Reset & Control

- PS_RESET_B (Zynq): Resets the processing system
- POR_B: Power-on reset input

FPGA hardware design: Programming & Debug

Programming & Debug

TCK, TMS, TDI, TDO: JTAG interface for programming and debugging

High-Speed I/O

- TXP/TXN, RXP/RXN: Differential transceiver pairs
- MGTAVCC / MGTAVTT: Power pins for multi-gigabit transceivers

FPGA hardware design: Analog System

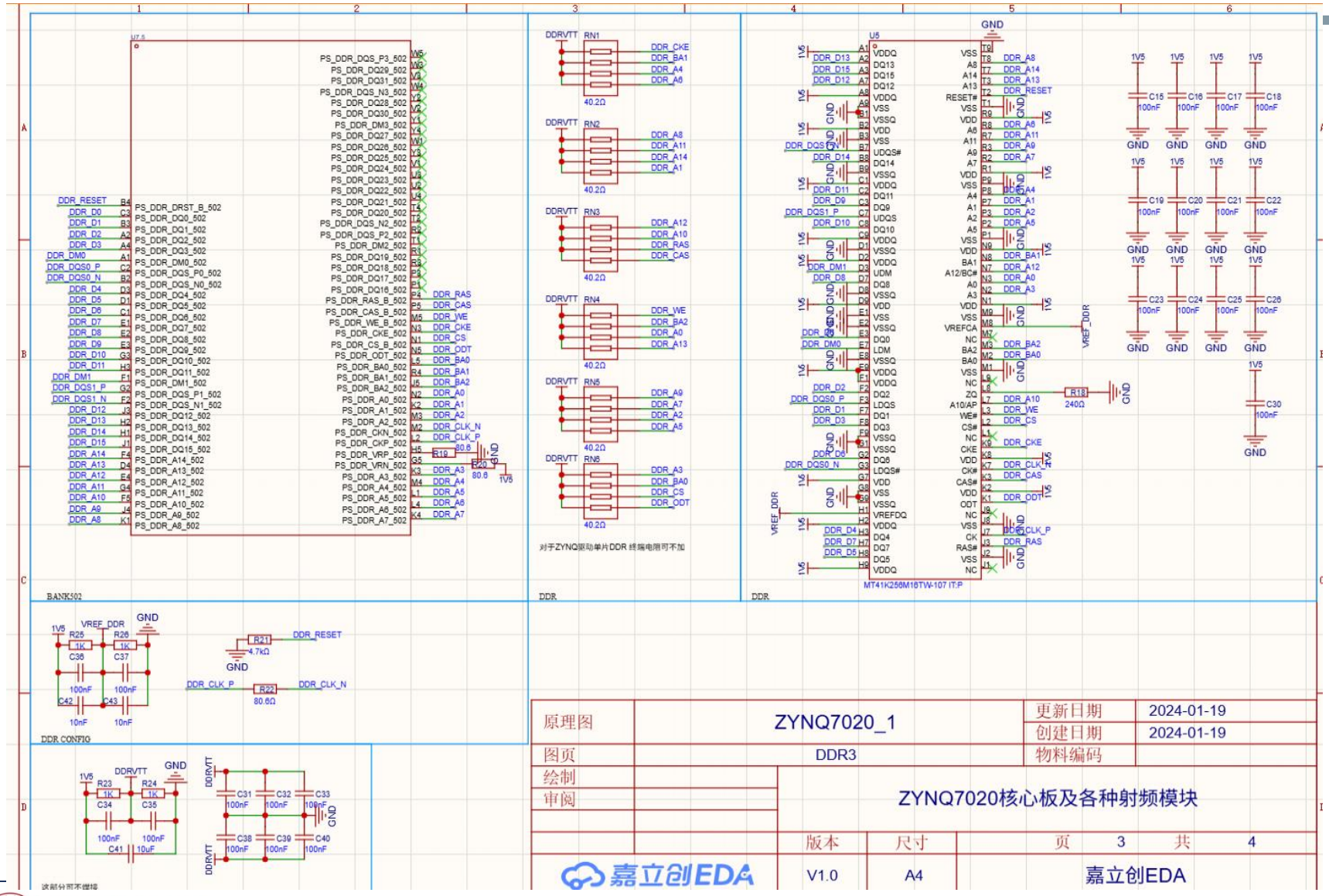
System Management

- VP / VN: Analog input pins for on-chip ADC (XADC)
- DXP / DXN: External temperature sensing inputs

Ground & Reference

- GND: Ground reference
- VREF: Reference voltage for certain I/O standards

FPGA hardware design: External RAM



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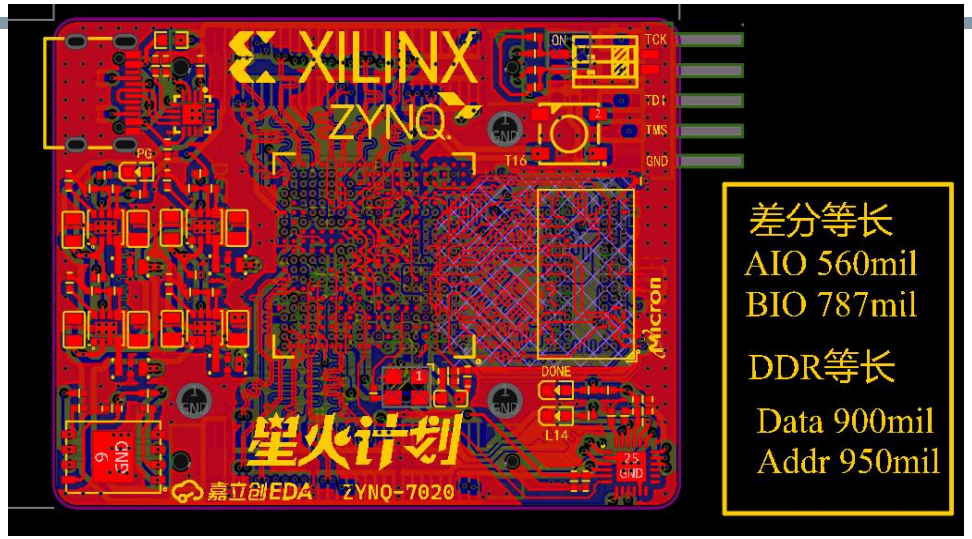
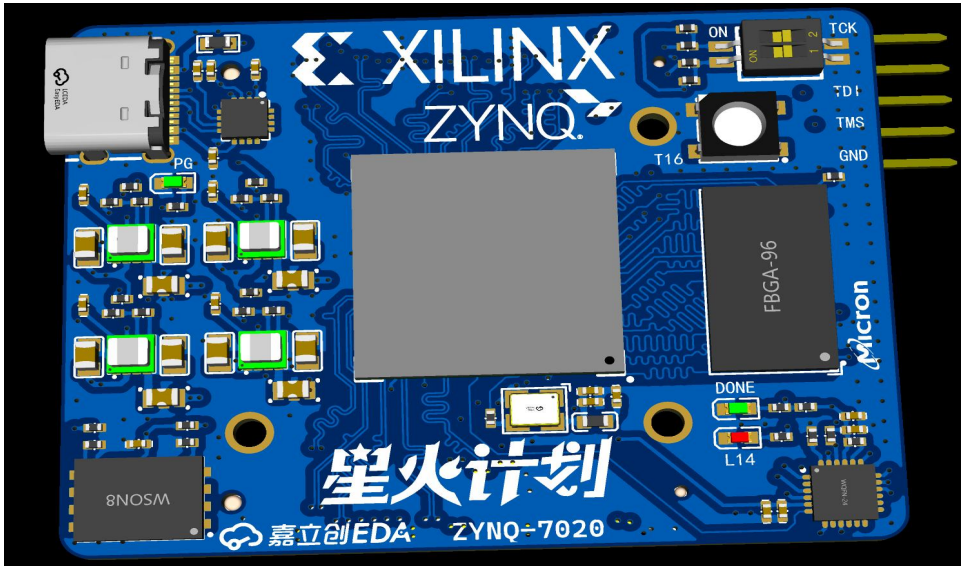
FPGA hardware design: PCB

- Connect to external circuits via diverse interfaces.
- High-speed signal integrity.
- Power & thermal.

- Take EE116 or electrical competition for more.





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References

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